IN THE CLAIMS

1. (Currently Amended): A circuit for detecting whether a telecommunication line is off-hook, said telecommunication line comprising tip and ring signal lines, said circuit comprising:

a voltage divider for coupling between said tip and ring lines and having a node at which is presented a scaled version of a voltage across said voltage divider;

a transistor having a control terminal coupled to said node and ~~first and second current flow terminals coupled between a voltage source and an output terminal~~ a first current flow terminal coupled to a voltage source and a second current flow terminal; and

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an analog-to-digital converter having an analog input and a digital output, said analog input coupled to said second current flow terminal of said transistor

~~whereby said output terminal bears a value that is indicative of the voltage across said tip and ring lines and thus whether said telecommunication line is off-hook.~~

2. (Currently Amended): The circuit of claim 1 wherein:

said voltage divider comprises a first resistor having a first terminal for coupling to said tip line and a second terminal coupled to said node and a second resistor having a first terminal for coupling to said ring line and a second terminal coupled to said node~~;~~.

3. (Cancelled).

4. (Currently Amended): The circuit of claim ~~3~~ 2 wherein said voltage of said voltage source is ground.

5. (Currently Amended): The circuit of claim ~~3~~ 2 further comprising:

a processor coupled to said digital output of said analog to digital converter, said processor adapted to determine whether said telecommunication line is off-hook based on a signal on said digital output of said analog to digital converter.

6. (Currently Amended): The circuit of claim ~~3~~ 2 wherein said analog to digital converter is a differential converter comprising first and second analog input terminals, said first analog input terminal coupled to said tip line and said second analog input terminal coupled to ring.

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7. (Original): The circuit of claim 6 further comprising a first capacitor coupled between said tip line and said first analog input terminal of said analog-to-digital converter and a second capacitor coupled between said ring line and said second analog input terminal of said analog to digital converter.

8. (Original): The circuit of claim 7 further comprising:

a diode having an anode coupled to said node and a cathode coupled to a control signal, said control signal having a first state which turns said diode on and drives said node to a voltage that turns said transistor off and a second state that turns said diode off whereby said node is driven to a voltage dictated by said voltage across said tip and ring lines.

9. (Currently Amended): A telecommunication apparatus for coupling to a telecommunication link, said telecommunication link comprising tip and ring lines at a first voltage when said link is on-hook and at a second voltage when said link is off-hook, said apparatus comprising:

a processor;

a first circuit for taking said apparatus off-hook so that said apparatus may receive or transmit information via said telecommunication link;

an analog-to-digital converter having an input terminal coupled to receive signals from said telecommunication link and having an output terminal coupled to said processor; and

a detection circuit for detecting whether said telecommunication link is off-hook, said detection circuit comprising:

a voltage divider for coupling between tip and ring and having a node at which is presented a scaled version of a voltage across said voltage divider; and

a transistor having a control terminal coupled to said node so as to be turned on or off responsive to a voltage across tip and ring, and ~~first and second current flow terminals coupled between a voltage source and said analog-to-digital converter~~ a first current flow terminal coupled to a voltage source and a second current flow terminal coupled to said input terminal of said analog-to-digital converter whereby, when said transistor is turned on, said analog-to-digital converter receives a first voltage

and, when said transistor is turned off, said analog-to-digital converter receives a second voltage; and

wherein said processor is adapted to disable said first circuit responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage.

10. (Original): The apparatus of claim 9 wherein:

said voltage divider comprises a first resistor having a first terminal for coupling to tip and a second terminal coupled to said node and a second resistor having a first terminal for coupling to ring and a second terminal coupled to said node.

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11. (Original): The apparatus of claim 10 wherein said analog-to-digital converter is a differential converter comprising first and second analog input terminals, said first analog input terminal coupled to tip and said second analog input terminal coupled to ring.

12, (Original): The circuit of claim 11 further comprising a first capacitor coupled between said tip line and said first analog input terminal of said analog to digital converter and a second capacitor coupled between said ring line and said second analog input terminal of said analog to digital converter.

13. (Original): The apparatus of claim 12 further comprising:

a diode having an anode coupled to said node and a cathode coupled to a control signal, said control signal having a first state which turns said diode on and

drives said node to a voltage that turns said transistor off and a second state that turns said diode off whereby said node is driven to a voltage dictate by said voltage across said tip and ring lines.

14. (Original): The apparatus of claim 13 wherein said control signal is normally in said first state and is switched to said second state just before said first circuit is to take said apparatus off-hook.

15. (Original): The apparatus of claim 14 wherein said signal is normally set to said first state and is momentarily set to said second state before said first circuit attempts to take said apparatus off-hook.

16. (Original): The apparatus of claim 15 further comprising:

a full wave rectifier circuit coupled between said detection circuit and said tip and ring lines.

17. (Original): The apparatus of claim 15 wherein said first and second inputs of said analog-to-digital converter are biased to common mode voltage.

18. (Currently Amended): The apparatus of claim 17 wherein said ~~fixed~~ voltage source is analog ground.

19. (Original): A circuit for detecting whether a telecommunication line is off-hook, said telecommunication line comprising tip and ring signal lines, said circuit comprising:

a voltage divider for coupling between said tip and ring lines and having first and second nodes across which appears a scaled version of a voltage across said tip and ring lines;

a differential analog-to-digital converter having first and second analog input terminals and a digital output terminal;

a signal line for selectively enabling said circuit when said signal is in a first state and disabling said circuit when said signal is in a second state;

a first transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said first node and said first input terminal of said analog-to-digital converter;

a second transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said second node and said second input terminal of said analog-to-digital converter;

whereby, when said signal line is in said first state, said analog-to-digital converter receives a scaled version of the voltage across said tip and ring lines and, when said signal line is in said second state, said analog-to-digital converter receives no signal from said voltage divider.

20. (Original): The circuit of claim 19 wherein:

said voltage divider comprises a first resistor having a first terminal coupled to said tip line and a second terminal coupled to said first node and a second resistor having a first terminal coupled to said first node ring and a second terminal coupled to said second node.

21. (Original): The circuit of claim 20 further comprising a diode coupled between said second node and said ring line.

22. (Original): The circuit of claim 20 further comprising:

a processor coupled to said digital output of said analog-to-digital converter, said processor adapted to determine whether said telecommunication line is off-hook responsive to a signal on said digital output of said analog-to-digital converter.

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23. (Original): A telecommunication apparatus for coupling to a telecommunication link, said telecommunication link comprising tip and ring lines that are biased to a first voltage when said link is on-hook and a second voltage when said link is off-hook, said apparatus comprising:

a processor;

a first circuit for taking said apparatus off-hook so that said apparatus may receive or transmit information via said telecommunication link;

a voltage divider for coupling between said tip and ring lines and having first and second nodes across which appears a scaled version of a voltage across said tip and ring lines;

a differential analog-to-digital converter having first and second analog input terminals and a digital output terminal;

a signal line for selectively enabling said circuit when said signal is in a first state and disabling said circuit when said signal is in a second state;

a first transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said first node and said first input terminal of said analog-to-digital converter;

a second transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said second node and said second input terminal of said analog-to-digital converter;

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whereby, when said signal line is in said first state, said analog-to-digital converter receives a scaled version of the voltage across said tip and ring lines and, when said signal line is in said second state, said analog-to-digital converter receives no signal from said voltage divider; and

said processor is adapted to disable said first circuit responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage.

24. (Original): The apparatus of claim 23 wherein:

said voltage divider comprises a first resistor having a first terminal coupled to said tip line and a second terminal coupled to said first node and a second resistor having a first terminal coupled to said first node ring and a second terminal coupled to said second node.

25. (Original): The circuit of claim 24 further comprising a diode coupled between said second node and said ring line.

26. (Original): The circuit of claim 24 further comprising:

a processor coupled to said digital output of said analog-to-digital converter, said processor adapted to determine whether said telecommunication line is off-hook responsive to a signal on said digital output of said analog-to-digital converter.

27. (Original): A method for detecting whether a telecommunication line is off-hook without affecting the line impedance, said telecommunication line comprising tip and ring signal lines, said method comprising the steps of:

(1) modulating a DC voltage that appears across said tip and ring lines;

(2) passing said modulated DC voltage through an electrical high voltage interface circuit; and

(3) determining whether said telecommunication line is off-hook as a function of said modulated DC voltage.

28. (Original): The method of claim 27 wherein step (1) comprises converting said DC voltage appearing across said tip and ring lines from analog to digital.

29. (Original): The method of claim 28 further comprising the step of:

(4) scaling said analog DC voltage appearing across said tip and ring lines before step (1).

30. (Original): The method of claim 29 wherein said DC voltage appearing across said tip and ring lines is scaled by a voltage divider.

31. (Original): The method of claim 27 wherein step (3) comprises comparing said modulated DC voltage to a reference value.

32. (Original): The method of claim 31 wherein step (3) is performed by a digital signal processor.

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33. (Original): The method of claim 29 further comprising the step of:

(5) selectively enabling said DC voltage appearing across said tip and ring lines to be modulated.

34. (Original): The method of claim 29 further comprising the steps of:

(6) converting said DC voltage to a two state signal indicative of said DC voltage before step (1).

35. (Original): The method of claim 34 wherein step (6) comprises controlling a transistor to turn on or off responsive to said DC voltage appearing across said tip and ring lines.